Clean Version

of

Substitute Specification Pages 8 and 9

for

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example, silicon dioxide, silicon nitride, silicon oxynitride, or the like, may be formed over the previously formed structures. One or more openings 122 (*e.g.*, vias or trenches) may be then etched through the insulating layer 120.

As illustrated in Figure 2, a barrier metal layer 202 (*e.g.*, titanium nitride, tantalum, tantalum nitride, or the like) may be deposited over the insulating layer 120 to inhibit migration of copper (deposited in a later process step) into silicon structures. A copper seed layer 204 may then be deposited over the barrier metal. Thereafter, a copper layer 206 may be deposited, typically by a electrolytic plating process, over the copper seed layer 204 to fill the openings 122 (Figure 1). This process typically produces the copper layer 206 across the entire wafer. Once a sufficiently thick copper layer 206 has been deposited, the copper layer 206 may be planarized using CMP techniques. In the example illustrated in Figures 1 and 2, the copper layer 206 is applied to the wafer to provide contacts 208 to source/drain regions 110. After planarizing the copper layer 206, further insulating layers (similar to the insulating layer 120) may be applied to the wafer, etched to form additional openings (*e.g.*, trenches and the like), and filled with copper to form electrical interconnections between the previously formed contacts and the like. Thus, the process of applying an insulating layer, etching the insulating layer to form openings, depositing a copper layer thereover, and planarizing the copper layer is repeated as desired to form multilevel metal schemes, such as dual damascene schemes.

It is generally advantageous to optimize the thickness of a copper layer (*e.g.*, the copper layer 206) so that the copper layer 206 is sufficiently thick to properly

conduct electrons as required and is sufficiently thin so that the time and materials required to planarize the copper layer are held to a minimum. Further, it is generally advantageous to optimize the thickness of the copper layer 206 on a wafer-by-wafer basis so that variations in thicknesses of copper layers (*e.g.*, the copper layer 206) on a series of wafers are minimized. Referring now to Figure 3, the illustrated embodiment comprises depositing a conductive layer (*e.g.*, the copper layer 206) on a wafer *J* (block 302), wherein *J* represents a wafer number in a series or lot of wafers. After the conductive layer has been deposited, the thickness of the conductive layer is measured (block 304) and is compared to a predetermined, acceptable thickness tolerance to determine if the thickness of the conductive layer is within acceptable limits (block 306). If the thickness of the conductive layer is not within tolerance, the deposition recipe is revised (block 308) so that the conductive layer on the next wafer (i.e., wafer *J*+1) will have a thickness that is within tolerance. The deposition recipe for an electroplating process controls, for example, the electroplating bath temperature, electroplating chemical concentrations, anode-cathode spacing, the anode power settings, the electroplating deposition time, and the like so that the electroplating process will give the desired thickness of the conductive layer. If, however, the thickness of the conductive layer is within tolerance, the next wafer (i.e., wafer *J*+1) is processed (blocks 310, 302) with no changes to the deposition recipe.